REMARKS

Claims 1-16, 24, 26, 27, 29, and 30 are all the claims pending in the application. Claims 1-16, 24, 26-27, and 29-30 stand rejected on prior art grounds. Applicants gratefully acknowledge that claims 25 and 28 would be allowable if rewritten in independent form. Accordingly, claims 1 and 9 are amended to incorporate the limitations of claims 25 and 28, respectively, and claims 25 and 28 are cancelled herein without prejudice or disclaimer. Claims 17-23 have been previously cancelled without prejudice or disclaimer. Applicants respectfully traverse the rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-16, 24, 26, and 29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wu, et al. (U.S. Publication No. 2004/0195628) hereinafter referred to as "Wu", in view of McCaldin, et al. (U.S. Patent No. 3,328,210), hereinafter referred to as "McCaldin". Claims 27 and 30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wu and McCaldin, in view of Collaert, et al. (U.S. Publication No. 2005/0020020), hereinafter referred to as "Collaert". Applicants respectfully traverse these rejections based on the following discussion.

Wu teaches a method of forming a FINFET CMOS device structure featuring an N channel device and a P channel device formed in the same SOI layer. The method features formation of two parallel SOI fin type structures, followed by gate insulator growth on the sides of the SOI fin type structures, and definition of a conductive gate structure formed traversing the SOI fin type structures while interfacing the gate insulator layer. A doped insulator layer of a first conductivity type is formed on the exposed top surfaces of a first SOI fin type shape, while a

second doped insulator layer of a second conductivity type is formed on the exposed top surfaces of the second SOI fin type shape. An anneal procedure results creation of a source/drain region of a first conductivity type in portions of the first SOI fin type shape underlying the first doped insulator layer, and creation of a source/drain region of a second conductivity type in portions of the second SOI fin type shape underlying the second doped insulator layer. Selective deposition of tungsten on exposed top surface of the source/drain regions is then employed to decrease source/drain resistance.

McCaldin teaches a process for treating insulation components of semiconductor devices to control or alter the properties of the insulation components as well as the material adjacent to the treated insulation components, whereby the treatment results in the distribution of a permanently induced space charge in the treated layer.

Collaert teaches a CMOS circuit for and method of forming a FinFET device is disclosed. The method includes providing a substrate comprising a semiconductor layer, forming on the semiconductor layer active areas insulated from each other by field areas, forming at least one dummy gate on at least one of said active areas and forming source and drain regions on the at least one of the active areas. The method also includes covering the substrate with an insulating layer leaving said dummy gate exposed and forming an open cavity by patterning the dummy gate to form a dummy fin and a semiconductor fin aligned to said dummy fin, both fins extending from the source to the drain regions.

However, the claimed invention, as provided in amended independent claims 1 and 9 contain features, which are patentably distinguishable from the prior art references of record. Specifically, claims 1 and 9 incorporate the limitations of claims 25 and 28, respectively (now

cancelled without prejudice or disclaimer), which the Office Action indicates includes allowable subject matter. Accordingly, claims 1 and 9 provide, in part, "...wherein each of said source and drain regions comprise a semiconductor layer comprising said alkali metal ion."

In view of the foregoing, the Applicants respectfully submit that the cited prior art references do not teach or suggest the features defined by amended independent claims 1 and 9 and as such, claims 1 and 9 are patentable over the cited prior art. Furthermore, dependent claims 2-8, 10-16, 24, 26, 27, 29, and 30 are similarly patentable over the cited prior art, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define. Thus, the Applicants respectfully request that these rejections be reconsidered and withdrawn.

Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being presented. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-16, 24, 26, 27, 29, and 30, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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Mohammad S. Rahman
Registration No. 43,029

Gibb I.P. Law Firm, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (301) 261-8625
Fax: (301) 261-8825
Customer Number: 29154